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SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION PTO-1449		 26615 PATENT TRADEMARK OFFICE	ATTORNEY'S DKT No. H1131		APPLICATION No. Unassigned 10/613,997			
			APPLICANT(S) Matthew S. BUYNOSKI et al.		FILING DATE July 8, 2003		GROUP Unassigned 2822	
U.S. PATENT DOCUMENTS								
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE		
MT	5,932,911	08/03/99	Yue et al.	257	330			
MT	6,180,441	01/30/01	Yue et al.	438	197			
FOREIGN PATENT DOCUMENTS								
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation		
						Yes	No	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)								
MT	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.							
MT	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.							
MT	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.							
MT	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.							
MT	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.							
EXAMINER			Michael Trinh		DATE CONSIDERED			12/8/03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).